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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,390	SPRACKLEN ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *58-61* is/are allowed.

6)☒ Claim(s) *1-3, 10-57, and 62-66* is/are rejected.

7)☒ Claim(s) *4-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/30/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 16-53 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims to computer-related inventions that are clearly nonstatutory fall into the same general categories as nonstatutory claims in other arts, namely natural phenomena such as magnetism, and abstract ideas or laws of nature which constitute "descriptive material. "Abstract ideas, Warmerdam, 33 F.3d at 1360, 31 USPQ2d at 1759, or the mere manipulation of abstract ideas, Schrader, 22 F.3d at 292-93, 30 USPQ2d at 1457-58, are not patentable. Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data (See MPEP section 2106, IV, B, 1).

Claim 16 comprises steps of tracking and predicting. The steps are just an abstract idea. The claim do not provide practical application that produces a useful, tangible and concrete result. Therefore, the claim is non-statutory. Similar problems exist in the other claims 28, and 38.

Claims 27, 37, and 47-53 are not limited to tangible embodiments. In view of Applicant's disclosure, specification page 18, paragraph [1063], lines 4-13, the machine-readable medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., CD-ROM) and intangible embodiments (e.g., carrier waves, infrared signals, and digital signals). As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

Drawings

3. The drawings are objected to because in Fig. 5D, the reference number of "Alias Prediction Register Bypass Encoding", "505" should read -507-. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the

replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities:

at page 6, line 1, "103" should read -105-;

at page 18, line 3, "705sends" should read -705 sends -;

at page 18, line 6, "705also" should read -705 also-.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. Claims 28-47, and 62-66 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 28, lines 7-9, it is not clear what is meant by "a dynamic identifier that corresponds to the read type instruction's dynamic identifier and the displacement" since it is not understandable. How can a dynamic identifier correspond to both the read type instruction's dynamic identifier and the displacement ? Something is missing in the claim language.

In claim 38, lines 9-10, it is not clear what is meant by "selecting a second write type instruction based at least in part on the displacement and the read type instruction" since it is not understandable. Something is missing in the claim language.

In claim 62, lines 7-18, it is not clear what is meant by "to indication said detections to the alias predictor" since it is not understandable. Besides, "said detections to the alias predictor" lacks proper antecedent basis since it was not described previously.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1-3, 10-47, 54-57, and 62-64 are rejected under 35 U.S.C. 102(a) as being anticipated by Shen et al., "*Modern Processor Design-Fundamentals of Superscalar Processors*", 2003, McGraw-Hill Higher Education, Beta edition, Chapter 4, pages 196-202., herein referred to as Shen et al.

Referring to claim 1, Shen et al. discloses, as claimed, a processor (Fig. 4-46) that predicts aliasing (see Page 201, lines 9-14, regarding alias prediction) between read type instructions (load instructions) and write type instructions (store instructions) based at least in part on respective displacements between the read type and write type instructions (such as the load and store instructions exist in a loop, see

Fig. 4-43) and on previous detection of respective aliasings between the read type instructions and the write type instructions, and that bypasses data (forward the store data directly to the load, see Fig. 4-43 (b)) from the write type instructions (store instructions) to the corresponding predicted to alias read type instructions (load instructions) using register information of the write type instructions.

Referring to claim 16, Shen et al. discloses, as claimed, a method comprising: in a register rename stage, tracking a write type instruction (store instruction) that has previously been indicated as aliased; and predicting (see Page 201, lines 9-14, regarding alias prediction) a read type instruction (load instructions) will alias with the write type instruction if displacement between the read type instruction and the write type instruction matches displacement between the read type instruction and a previously aliased write type instruction (such as the load and store instructions exist in a loop, see Fig. 4-43).

Referring to claim 28, Shen et al. disclose, as claimed, a method (see Fig. 4-46) comprising: observing repeated aliasing (such as the load and store instructions exist in a loop, see Fig. 4-43) between a first write type instruction (a first store instructions) and a read type instruction (load instructions)

based at least in part on their static identifiers (such as the pointers for each program saved in a memory); determining a displacement (such as the load and store instructions exist in a loop, see Fig. 4-43) between the first write type instruction (store instructions) and the read type instruction based on dynamic identifiers (see Fig. 4-46, the addresses in store and load units) of the instructions; predicting aliasing (see Page 201, lines 9-14, regarding alias prediction) between the read type instruction (load instructions) as identified by the static identifier (such as the pointers for each program saved in a memory) thereof and a second write type instruction (a second store instruction) identified with a dynamic identifier (see Fig. 4-46, the addresses in store and load units) that corresponds to the read type instruction's dynamic identifier (see Fig. 4-46, the addresses in store and load units) and the displacement.

Referring to claim 38, Shen et al. disclose, as claimed, a method comprising: detecting aliasing (see Page 201, lines 9-14, regarding alias prediction) between a read type instruction and a first write type instruction; determining displacement (such as the load and store instructions exist in a loop, see Fig. 4-43) between the read type instruction and the first write type instruction, wherein the displacement is with respect to program

execution; observing repeated aliasing between the read type instruction and the first write type instruction; selecting a second write type instruction based at least in part on the displacement and the read type instruction; and bypassing data (forward the store data directly to the load, see Fig. 4-43 (b)) from the second write type instruction's data source to the read type instruction's data Destination (see claims 1 and 28 as set forth above).

Referring to claim 54, Shen et al. discloses, as claimed, an apparatus comprising: a data hazard detection module (see Fig. 4-46); and means for predicting (see Page 201, lines 9-14, regarding alias prediction) aliasing between a read type instruction (load instructions) and a first write type instruction (a first store instruction) based on displacement (such as the load and store instructions exist in a loop, see Fig. 4-43) between the instructions and previously observed aliasing between the read type instruction (load instructions) and a second write type instruction (a second store instruction), wherein the read type instruction (load instructions) and the second write type instruction also have the same displacement.

Referring to claim 62, Shen et al. disclose, as claimed, an apparatus comprising: an alias predictor (inside the Shen et

al.'s system, see Page 201, lines 9-14, regarding alias prediction), including one or more encodings to host indications of particular instances of write type instructions (store instruction) and particular instances of read type instructions (load instructions), respective execution displacements (such as the load and store instructions exist in a loop, see Fig. 4-43) between respective ones of the particular instances of read and write type instructions, and register information of the particular write type instruction instances, to predict aliasings between read and write type instruction instances based, at least in part, on the encodings and indications of detected aliasings between the instruction instances; a rename unit (inside the Shen et al.'s system, see Fig. 4-46) coupled with the alias predictor, the rename unit to supply register information for write type instruction instances to the alias predictor; and a data hazard detection unit (inside the Shen et al.'s system, see Fig. 4-46) coupled with the alias predictor, the data hazard detection unit to detect aliasing between particular instances of read and write type instructions (such as the load and store instructions exist in a loop, see Fig. 4-43) and to indication said detections to the alias predictor.

As to claim 2, Shen et al. also discloses: the processor of claim 1 wherein the data is bypassed (forward the store data directly to the load, see Fig. 4-43 (b)) if a threshold number of repeated aliases are detected between read type instructions and write type instructions with the respective displacements (as set forth, this is in the situation such as the load and store instructions exist in a loop, see Fig. 4-43).

As to claim 3, Shen et al. also discloses: the processor of claim 1 that includes encodings of read type instruction information, write type instruction information, and repeat aliasing (see Page 199, lines 10-11, regarding the additional priority encoding logic).

As to claim 10, Shen et al. also discloses: the processor of claim 1 wherein data bypasses comprise the processor substituting a register move instruction for the read type instruction (since Shen et al.'s system forwarding the store data directly to the load, see Fig. 4-43 (b)).

As to claim 11, Shen et al. also discloses: the processor of claim 10, wherein a loadCheck instruction is inserted, which when executed by the processor, causes the processor to verify the predicted aliasing (see page 199, lines 6-12, regarding the alias detection must be exact before forwarding of the data can

be performed). Note LoadCheck is just a name without having any patentable weight.

As to claim 12, Shen et al. also discloses: the processor of claim 10 wherein the register move instruction includes an integer-to-integer move instruction, a floating point-to-floating point move instruction, an integer-to-floating point move instruction, and a floating point-to-integer move instruction (note the above are the situations of forwarding data between floating point-to-floating point, integer-to-floating point, and a floating point-to-integer).

As to claim 13, Shen et al. also discloses: the processor of claim 1 wherein data bypasses comprise the processor mapping the read type instruction's destination register to the write type instruction's source register (see Fig. 4-46 regarding Tag match).

As to claim 14, Shen et al. also discloses: the processor of claim 13 that replaces the read type instruction with a loadCheck instruction, which when executed by the processor, causes the processor to verify the predicted aliasing (see page 199, lines 6-12, regarding the alias detection must be exact before forwarding of the data can be performed). Note LoadCheck is just a name without having any patentable weight..

As to claim 15, Shen et al. also discloses: the processor of claim 14 wherein the processor's verification of the predicted aliasing comprises interrogation of a data hazard detection module (inside the Shen et al.'s system, see page 199, lines 6-12, regarding the alias detection must be exact before forwarding of the data can be performed) to ascertain whether addresses of the write type instruction and the read type instruction predicted to alias with the write type instruction match (see Fig. 4-46 regarding Tag match), and verification of absence of intervening matching write type instructions.

As to claim 17, Shen et al. also discloses: the method of claim 16 wherein the displacement is measured with dynamic instruction identifiers (see Fig. 4-46, the addresses in store and load units), wherein the dynamic instruction identifiers identify instances of instructions with respect to program execution.

As to claim 18, Shen et al. also discloses: the method of claim 16 wherein the write type instruction and the read type instruction are tracked with their static identifier (such as the pointers for each program saved in a memory), wherein the static identifier identifies an instruction in a program and remains static during program execution.

As to claim 19, Shen et al. also discloses: the method of claim 18 wherein the static identifier (such as the pointers for each program saved in a memory), includes an instruction address (since a pointer can be an address).

As to claim 20, Shen et al. also discloses: the method of claim 16 wherein a read type instruction (load instruction) includes a load instruction, a load halfword instruction, a load byte instruction , a load float instruction, a load double instruction, and a load multiple instruction (note the above are just the different instruction types).

As to claim 21, Shen et al. also discloses: the method of claim 16 wherein the write type instruction (store instruction) includes a store instruction, a store byte instruction, a store float instruction, a store double instruction, a store multiple instruction, and a store halfword instruction (note the above are just the different instruction types).

As to claim 22, Shen et al. also discloses: the method of claim 16 further comprising bypassing data (forward the store data directly to the load, see Fig. 4-43 (b)) of the write type instruction to the read type instruction with register information of the write type instruction.

As to claim 23, Shen et al. also discloses: the method of claim 22 wherein bypassing comprises mapping the read type

instruction's destination register to the write type instruction's source register (see claim 13 as set forth above).

As to claim 24, Shen et al. also discloses: the method of claim 23 further comprising replacing the read type instruction with a loadCheck instruction, wherein the loadCheck instruction causes interrogation of a data hazard detection module to ascertain whether addresses of the write type instruction and the read type instruction predicted to alias with the write type instruction match, and to ascertain whether there are any intervening matching write type instructions (see claims 14 and 15 as set forth above).

As to claim 25, Shen et al. also discloses: the method of claim 22 wherein bypassing comprises converting the read type instruction to a register move instruction (see claim 10 as set forth above).

As to claim 26, Shen et al. also discloses: the method of claim 25 further comprising inserting a loadCheck instruction, wherein the loadCheck instruction causes interrogation of a data hazard detection logic to ascertain whether addresses of the write type instruction and the read type instruction predicted to alias with the write type instruction match, and to ascertain whether there are any intervening matching write type instructions (see claims 14 and 15 as set forth above).

As to claim 27, Shen et al. also discloses: the method of claim 16 embodied as a computer program product encoded in one or more machine-readable media (such as the main memory of the Shen et al.'s system).

As to claim 29, Shen et al. also discloses: the method of claim 28 further comprising bypassing data of the second write type instruction to the read type; instruction with register information of the second write type instruction (see claim 1 as set forth above).

As to claim 30, Shen et al. also discloses: the method of claim 29 wherein bypassing the data comprises mapping the data source of the read type instruction to the data source of the write type instruction (see claim 13 as set forth above).

As to claim 31, Shen et al. also discloses: the method of claim 30 further comprising substituting a loadCheck instruction for the read type instruction, wherein execution of the loadCheck instruction causes interrogation of a data hazard detection module to ascertain whether addresses of the read type instruction and the second write type instruction match (see claims 14 and 15 as set forth above).

As to claim 32, Shen et al. also discloses: the method of claim 31 wherein execution of the loadCheck instruction further causes verifying the absence of intervening matching write type

instructions (note this is certainly included in the steps for detecting or checking the instructions).

As to claim 33, Shen et al. also discloses: the method of claim 29 wherein bypassing the data comprises substituting a register move instruction for the read type instruction, wherein the move instruction moves data from the data source of the write type instruction to the data destination of the read type instruction (see claim 10 as set forth above).

As to claim 34, Shen et al. also discloses: the method of claim 28 wherein the dynamic identifiers (see Fig. 4-46, the addresses in store and load units) monotonically increase with execution of a program that includes the instructions (since the instruction addresses are allocated increasingly in a memory).

As to claim 35, Shen et al. also discloses: the method of claim 28 wherein the static identifiers include instruction addresses (see claim 19 as set forth above).

As to claim 36, Shen et al. also discloses: the method of claim 28 wherein the aliasing is predicted if the number of observed repeat aliasings exceeds a threshold (this is in the situation such as the load and store instructions exist in a loop, see Fig. 4-43).

As to claim 37, Shen et al. also discloses: the method of claim 28 embodied as a computer program product encoded in one

or more machine-readable media (such as the main memory of the Shen et al.'s system).

As to claim 39, Shen et al. also discloses: the method of claim 38 further comprising verifying that the second write type instruction (the second store instruction) aliases with the first read type instruction (the first load instruction).

As to claim 40, Shen et al. also discloses: the method of claim 38 wherein data bypass comprises changing the read type instruction to a register move instruction (see claim 10 as set forth above).

As to claim 41, Shen et al. also discloses: the method of claim 40 further comprising inserting a loadCheck instruction, wherein the loadCheck instruction causes verification that the read type instruction and the second write type instruction alias and verification of the absence of one or more intervening write type instructions (see claims 11 and 32 as set forth above).

As to claim 42, Shen et al. also discloses: the method of claim 38 wherein data bypasses comprise mapping the read type instruction's architectural destination register to the second write type instruction's rename source register (see claim 13 as set forth above).

As to claim 43, Shen et al. also discloses: the method of claim 42 further comprising changing the read type instruction to a IoadCheck instruction, wherein the loadCheck instruction causes verification that the read type instruction and the second write type instruction alias and verification of the absence of one or more intervening write type instructions (see claims 11 and 32 as set forth above).

As to claim 44, Shen et al. also discloses: the method of claim 38 wherein the first and second write type instructions have a same static identifier (such as the pointers for each program saved in a memory) and different dynamic identifiers (see Fig. 4-46, the addresses in store and load units since addresses in store and load units are changeable during the execution).

As to claim 45, Shen et al. also discloses: the method of claim 44 wherein the static identifiers (such as the pointers for each program saved in a memory) include instruction addresses (since a pointer can be an address).

As to claim 46, Shen et al. also discloses: the method of claim 38 wherein the displacement is based at least in part on the dynamic identifiers of the instructions, wherein the dynamic identifiers monotonically increase with execution of a program

that includes the instructions (see claim 34 as set forth above).

As to claim 47, Shen et al. also discloses: the method of claim 38 embodied as a computer program product encoded in one or more machine-readable media (such as the main memory of the Shen et al.'s system).

As to claim 55, Shen et al. also discloses: the apparatus of claim 54 further comprising means for bypassing data (forward the store data directly to the load, see Fig. 4-43 (b)) from the write type instruction to the read type instruction with register information of the write type instruction.

As to claim 56, Shen et al. also discloses: the apparatus of claim 54 wherein the read type instruction includes a load instruction, a load halfword instruction, a load byte instruction, a load float instruction, a load double instruction, and a load multiple instruction (see claim 20 as set forth above).

As to claim 57, Shen et al. also discloses: the apparatus of claim 54 wherein the write type instruction includes a store instruction, a store byte instruction, a store float instruction, a store double instruction, a store multiple instruction, and a store halfword instruction (see claim 21 as set forth above).

As to claim 63, Shen et al. also discloses: the apparatus of claim 62, wherein the indications of particular instances of instructions include instruction instance addresses (see Fig. 4-46, the addresses in store and load units; and such as the pointers for each program saved in a memory).

As to claim 64, Shen et al. also discloses: the apparatus of claim 63, wherein the instruction instances addresses include one or more of static identifiers (such as the pointers for each program saved in a memory) and dynamic identifiers (see Fig. 4-46, the addresses in store and load units).

Allowable Subject Matter

8. Claims 58-61 are allowed.

9. Claims 4-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 65 and 66 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph,

set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: Shen et al., the closest reference, and the other prior art do not teach or fairly suggest: the instruction rename to track read type instructions indicated by the data hazard detection module as aliasing and repeat aliasing of the tracked read type instructions, and to indicate displacements between the tracked read type instructions and aliased write type instructions (in claim 58).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Feiste et al. discloses forwarding store instruction result to load instruction with reduced stall or flushing by effective/real data address bytes matching. When a store instruction has already been translated, the load address range of a load instruction is contained within the address range of the store instruction, and the data associated with the store instruction is available, then the data associated with the

store instruction is forwarded to the load instruction so that the load instruction may continue execution without having to be stalled or flushed.

Papworth et al. discloses a method and apparatus for dynamically allocating entries of microprocessor resources to particular instructions in an efficient manner to efficiently utilize buffer size and resources. The pipelined and superscalar microprocessor is capable of speculatively executing instructions and also out-of-order processing.

Tran et al. discloses a microprocessor including a reorder buffer configured to store speculative register values regarding a particular register is provided. One value is stored for each set of concurrently decoded instructions which are outstanding within the microprocessor, reflecting the updates of each instruction within the set which updates the register.

Contact Information

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Fritz M. Fleming, can be reached on (571) 272-4145. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

14. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 571-273-8300.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
May 31, 2006